A Physically-Based Transient *SPICE* Model for GaAs MESFET's

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***Abstract*—A physically-based transient *SPICE* model was developed for GaAs MESFET's. The model accounts for both trapping and detrapping effects hence can simultaneously simulate low-frequency dispersion and gate-lag characteristics. This is different from conventional models which can simulate either effect but not both. The present model was verified in terms of pulsed *I-V* characteristics and digitally-modulated RF carrier waveforms.**

I. Introduction

For efficient design of RF power amplifiers in digitally-modulated wireless applications, it is important to develop a large-signal transistor model that is capable of predicting the device behavior over a wide range of time scales and biasing conditions. Since a general model which accounts for all past state variables is too cumbersome to be useful, approximation and simplification are necessary. To date low-frequency dispersion models have been developed [1], [2] to account for the differences between RF and dc modes of operation. However, this type of model neglects the transient effects of digital modulation.

The transient response of GaAs MESFET's at approximately 1 μs and longer are mainly due to surface and bulk traps [1], with surface traps dominating in devices fabricated on epitaxial material [3]. The surface traps can cause gate lag [4] in addition to low-frequency dispersion. Gate lag is associated with a change in trap occupation over time while dispersion is determined by the steady-state trap response for a given excitation. The steady-state response is the result of a balance between trapping and detrapping. Therefore, by adding simple charging and discharging subcircuits to a conventional MESFET model, low-frequency dispersion and gate lag can be simultaneously simulated. In the following, we describe the implementation of such subcircuits in a SPICE-based MESFET model. Using this model, transients of RF carrier waveforms under digital modulation were successfully simulated for the first time.

II. Model Construction

The present model was extracted from a MESFET fabricated on GaAs grown by vapor-phase epitaxy. The MESFET has a gate length and width of 0.3 and 300 μm, respectively. Its saturated and maximum drain currents are approximately 100 and 170 mA/mm, respectively. The threshold voltage is -1.75 V.

Pulsed *I-V* measurement (Fig. 1) was used to characterize the MESFET. The device was normally biased on long enough to bring the trap occupation to a steady state. Once every second the gate-source voltage was brought below threshold for different durations. The transient response after the device was turned back on was then measured. This measurement was repeated with on voltages of -0.5, 0.0, and 0.5 V, off voltages of -4, -3, and -2 V, and off times of 0.01, 0.1 ... 100 ms. From the dependencies of on and off times the trap charging and discharging rates are inferred. Fig. 2 shows the drain current as a function of time after the gate-source voltage was pulsed from 0.5 V to -4 V for different durations.

The instantaneous drain current i_{DS} can be fit to Eq. (1), where I_{DS} is the steady-state current; α_J denotes the fractional change of drain current due to the J-type of traps; t_{OFF} is the duration spent below pinch-off; τ_C is the charging time constant; t is the time after the pulse; τ_D is the discharging time constant. Usually only three sets of τ_C and τ_D are required. Notice that the effects of off-state drain-source and gate-source voltages are such that they can be lumped together as a single parameter in terms of off-state drain-gate voltage. Fig. 3 shows that τ_C and τ_D are approximately constant over a wide range of off drain-gate voltages. Fig. 4 shows that α_J is approximately a linear function of off drain-gate voltage. Thus, the complicated historical dependence of i_{DS} can be greatly simplified making Eq. (1) sufficiently compact for circuit simulation use.

Fig. 5 shows the drain characteristics at t = 1 μs and 0.5 s (steady state), respectively, after the MESFET was pulsed back on. Transients are apparent in terms of increased linear resistance and decreased saturated current. Using *SPICE*, the increase in drain resistance can be implemented through a MESFET operating in the linear region while the decrease in drain current can be implemented through a voltage-dependent current source as shown in Fig. 6. Time dependent control of the parasitic MESFET and current source is provided by a set of three nonlinear *RC* subcircuits driven by the drain-gate voltage (Fig. 7). One subcircuit is needed for each set of charging/discharging times. With unity capacitance, $RC = \tau_C$ and $R_D = \tau_D$. Diodes in the subcircuit ensure the direction of charge flow. The instantaneous voltage across the capacitor is then used to control the parasitic MESFET and current source. The intrinsic MESFET can be simulated by a conventional model such as the *SPICE* Level 1 Curtice model. Fig. 5 compares the simulated and measured characteristics of the intrinsic MESFET.

$$i_{DS}\left(V_{DS}, V_{GS}, t, V_{DG}^{OFF}, t_{OFF}\right) = I_{DS}\left(V_{DS}, V_{GS}\right)\left[1 - \sum_{J=1,2,3} \alpha_J\left(V_{DG}^{OFF}\right) \cdot \left(1 - e^{-\frac{t_{OFF}}{\tau_C^J}}\right) \cdot e^{-\frac{t}{\tau_D^J}}\right] \quad (1)$$

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III. Model Verification

For model verification, pulsed *I-V* characteristics after various combinations of off voltages and times were simulated and compared to the measured results (Fig. 8). To verify the model further, two additional experiments were run. In the first experiment, the MESFET was normally biased off for sufficient time to ensure a steady off state. It was then pulsed on, with a 7 KHz, 1.5 V ac signal superimposed on the pulse (Fig. 9). In the second experiment, the MESFET was normally biased on to ensure a steady on state. It was then pulsed down to partially off, with a 100 KHz, 1.25 V ac signal superimposed on the pulse (Fig. 10). compares the simulated and measured results in this case. In general, the simulated results compare well with the measured data.

IV. Discussion

The success of the present model in simulating the transient behavior of a MESFET after various historical events is primarily owing to the use of both charging and discharging time constants. While the general supposition has been that the average voltages are what determine a device's high-frequency response [1], the above simulations and measurements show that this supposition is not necessarily valid. This is because the balance between trapping and detrapping at steady state is history dependent. In fact, in some cases the extreme voltages are more consequential than the average voltages.

Due to the modest bias conditions, the present device has well behaved charging and discharging time constants. If biased more aggressively, it is possible for impact ionization to drastically affect charging and discharging rates [5] which will require more precise treatment of impact ionization.

While no high-frequency verification has been performed, the general agreement between the simulated and measured results at lower frequencies indicate that the model will be capable of predicting the transient of RF carrier waveforms for narrow-band applications. Simulating the transient of RF waveforms is computationally intensive due to the large differences between RF periods and detrapping times. By using an ac period approximately one tenth of the fastest trapping time and by properly scaling the capacitances and inductances, it is possible to achieve good agreement between the simulated ac response and the RF waveforms sampled at the same ac frequency, effectively aliasing RF with ac.

V. Conclusion

A physically-based transient *SPICE* model was developed to account for the charging and discharging of surface traps in epitaxial GaAs MESFET's. The ability to mimic trapping/detrapping through nonlinear *RC* circuits allows both low-frequency dispersion and gate-lag characteristics to be simulated simultaneously. With this flexibility the model is capable of simulating the transient of RF carrier waveforms under digital modulation. This model can be readily extended to include bulk traps in ion-implanted MESFET's.

References

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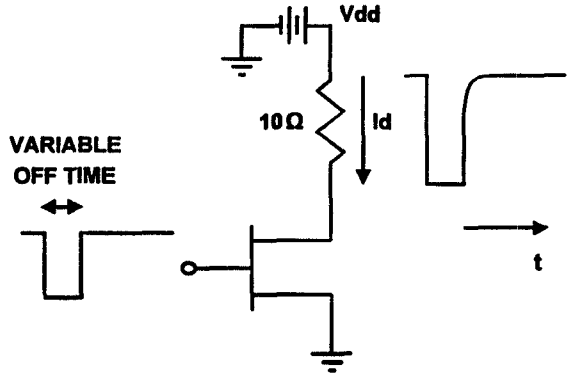


Fig. 1 Schematic of pulsed *I-V* measurement.

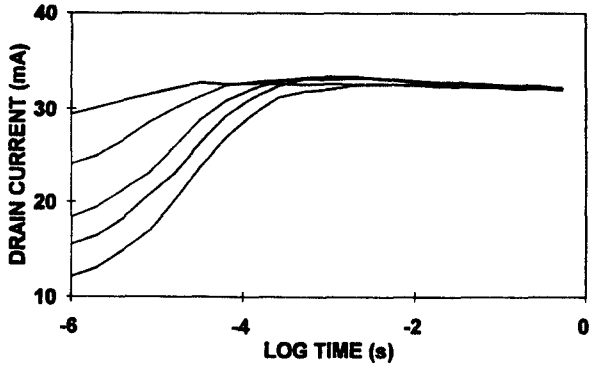
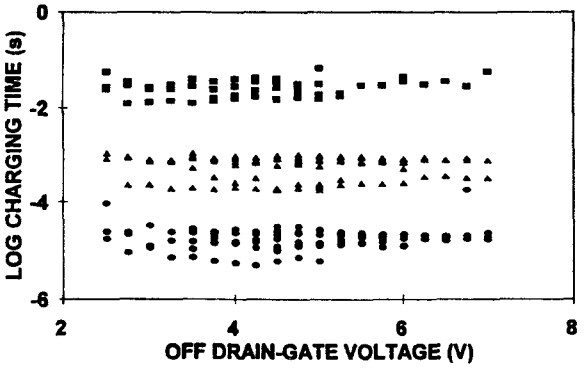
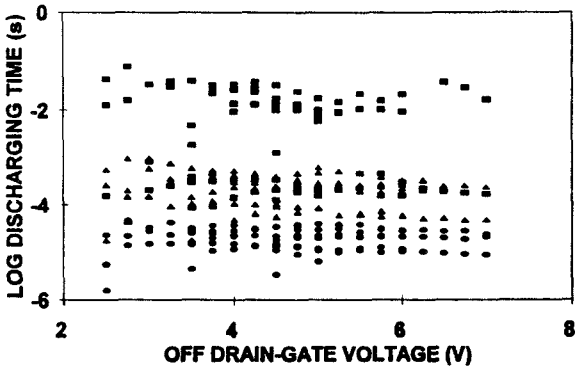


Fig. 2 MESFET transient response with time spent below pinch off as a parameter (0.01, 0.1 ... 100 ms top to bottom) for drain supply, on, and off gate-source voltages of 1, 0.5, and -4 V respectively.



(a)



(b)

Fig. 3 Three (a) charging and (b) discharging time constants extracted from pulsed *I-V* characteristics. Both sets of time constants are independent of off drain-gate voltage.

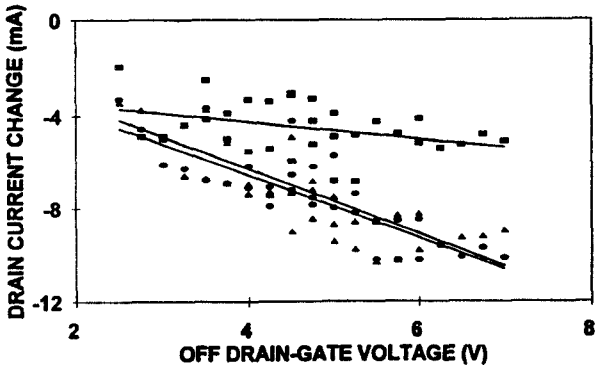


Fig. 4 Extracted drain current drop associated with discharging time constants of the order of (■) μs, (●) ms, and (▲) s. On gate-source voltage of 0.5 V.

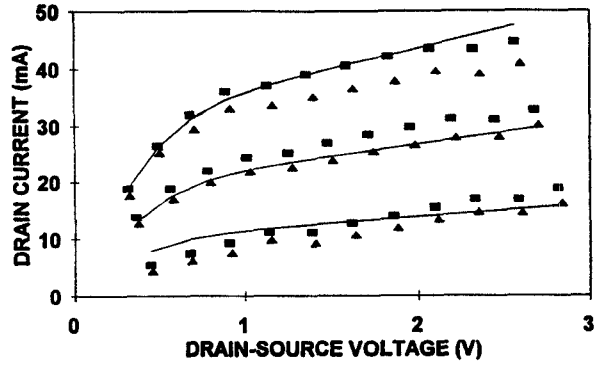


Fig. 5 Drain characteristics measured at (▲) 1μs and (■) 0.5 s after the device returns from pulsing to -4 V for 10 μs. (—) Simulated 0.5 s data using Curtice model. *Vgs*=-0.5, 0.0, and 0.5 V bottom up.

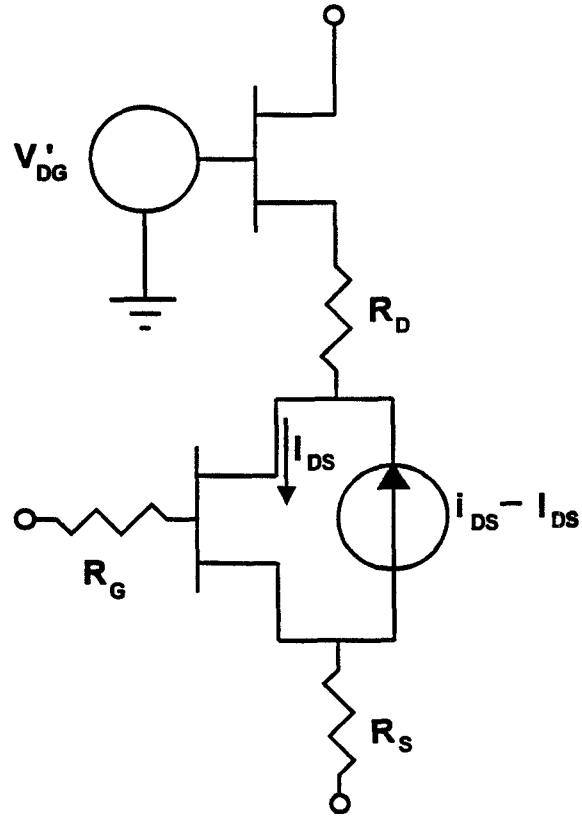
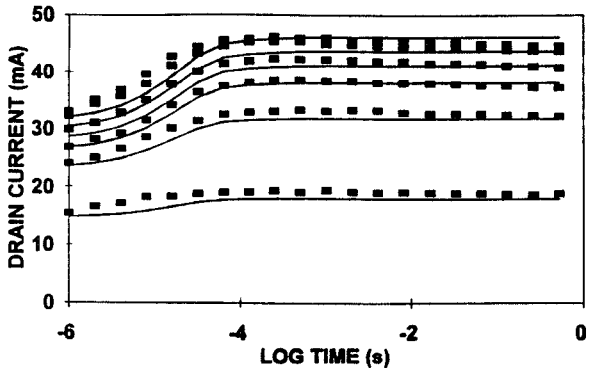
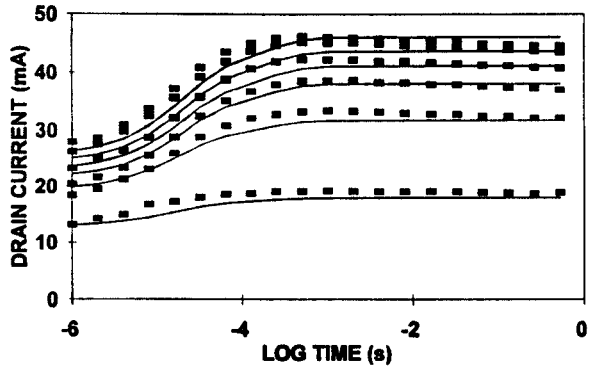


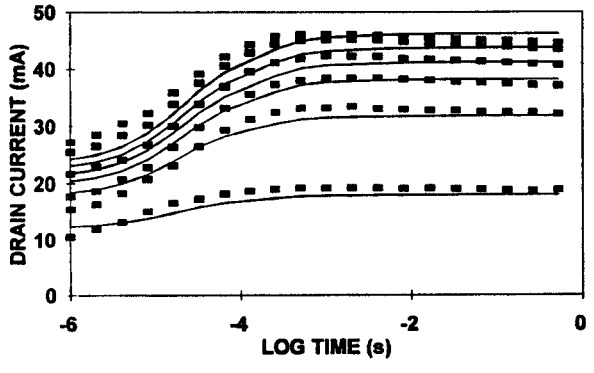
Fig. 6 Circuit model implemented in *SPICE*. Parasitic MESFET and current source are used to increase the drain resistance and decrease the saturated current, respectively.



(a)



(b)



(c)

Fig. 8 (■) Measured and (—) simulated drain current transients for off times of (a) 0.1, (b) 1, and (c) 10 ms. On and off gate-source voltages are 0.5 and −4 V. *Vdd*=0.5, 1.0 ... 3.0 V bottom up.

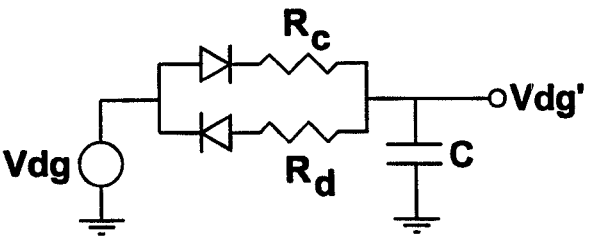


Fig. 7 Nonlinear *RC* subcircuit used to provide the temporal control of the voltage dependent parasitic MESFET and current source shown in Fig. 6. Instantaneous drain-gate voltage is used to drive the subcircuit.

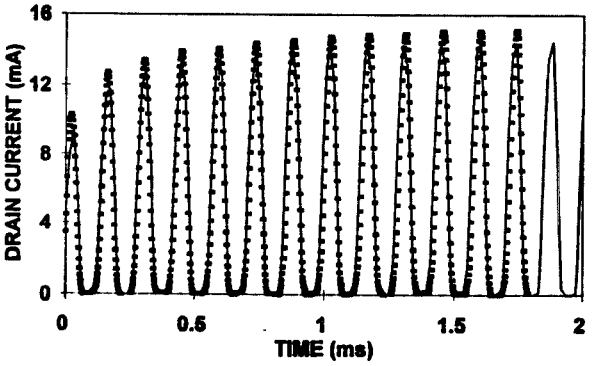


Fig. 9 (■) Measured and (—) simulated drain current response of a normally off MESFET to a gate pulse with a 7 KHz, 1.5 V ac signal superimposed on the pulse.

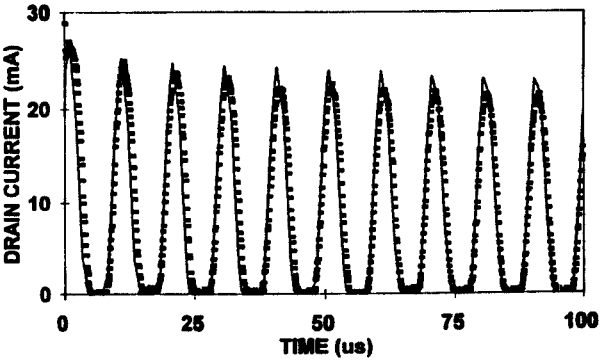


Fig. 10 (■) Measured and (—) simulated drain current response of a normally on MESFET to a gate pulse with a 100 KHz, 1.25 V ac signal superimposed on the pulse.